AMENDMENTS TO THE SPECIFICATION

In the Specification:

Please amend the paragraph beginning on page 1, line 11, as follows:

-- Recently, with increased integration of ~~a~~ semiconductor devices, ~~a~~ limit results have been achieved in connection with decreasing ~~the~~ line widths using ~~a~~ photolithography processes~~, which is used in semiconductor manufacturing processes~~. To solve the above-mentioned problem, a damascene process has been used. --

Please re-amend the paragraph beginning on page 1, line 20, as follows:

-- In the self-aligned dual damascene process, a via connecting the lower and upper interconnection lines is aligned at a bottom of the trench. That is, in the self-aligned dual damascene process, an insulating layer is selectively etched with a photolithography process to form a trench exposing a via at the bottom thereof, and a conductive layer is formed with W, Al or Cu to fill the trench. After that, a portion of the conductive layer outside of the trench, which is not needed, is removed by an etching or a chemical mechanical polishing (CMP) to form an interconnection line in the trench. --

Please amend the paragraph beginning on page 2, line 1, as follows:

-- The above-mentioned self-aligned dual damascene process is mainly used for forming a bit line, a word line and a metal interconnection line of a dynamic random access memory (DRAM). Specifically, by using a ~~the~~ self-aligned dual damascene process for forming ~~the~~ a trench, a via hole that is used to form a via connecting upper and lower interconnection lines~~,~~ may be formed simultaneously. By

using the self-aligned dual damascene process, a height difference due to the interconnection lines may is not be generated, since the via and interconnection lines are buried in the interlayer insulating layers. --

Please re-amend the paragraph beginning on page 4, line 10, as follows:

-- A method for forming multi-level interconnection lines using a dual damascene process is disclosed. With the dual damascene process, it is easy to control distortion of a profile of a corner of a trench, and to prevent the capacitance value from increasing due to a remaining ~~or intact~~ portion of the etching stop layer. --

Please amend the paragraph beginning on page 5, line 2, as follows:

-- Other aspects of the disclosed methods will become apparent from the following description with reference to the accompanying drawings, ~~aherein~~ wherein: --

Please re-enter the paragraph beginning on page 5, line 5, as follows:

-- Figs. 1A to 1D are cross-sectional views illustrating a conventional method of manufacturing metal interconnection lines using a dual damascene process; --

Please re-amend the paragraph beginning on page 5, line 27, as follows:

-- Referring to Fig. 3A, in a method of manufacturing multi-level metal interconnection lines, interlayer insulating layers 32 and 33 and an etching stop layer 34 are formed on a semiconductor substrate 31. After that, the etching stop layer 34

and the interlayer insulating layer 33 are selectively etched to ~~expose~~ form a via or a trench where a metal interconnection line 35 is then formed. --

Please amend the paragraph beginning on page 6, line 1 as follows:

-- Subsequently, a metal layer is deposited on the ~~exposed part~~ resultant structure and is then selectively removed to form a metal interconnection line 35 that extends ~~in~~ through the etching stop layer 34 and the interlayer insulating layer 33 as shown in Fig. 3A. --

Please re-amend the paragraph beginning on page 6, line 32 as follows:

-- Referring to Fig. 3C, after removing the via hole mask 38, another photoresist layer is coated on a resulting structure and is exposed and developed to form a photoresist pattern 40 covering the etching stop layer 37a that surrounds the via hole 39 (see Fig. 3B). The width d_1 of the photoresist pattern 40 is larger than that of a trench to be formed later, by as much as 0.2 μm to 1.0 μm, which is a minimum size needed for a subsequent etching process for forming an upper trench as shown in Figs. 3D and 3E. --

Please re-amend the paragraph beginning on page 7, line 8 as follows:

-- Returning to Fig. 3C, the etching stop layer 37 is etched using the photoresist pattern as an etch mask to form an etching stop pattern 37a around the via hole. That is, only the etching stop pattern 37a is left intact ~~where~~ where it can be used to form an upper trench as explained later in connection with Figs. 3D and 3E. Therefore, even if the etching stop pattern 37a is formed with a layer having high

dielectric constant, such as a ~~nitrogen~~ nitride layer, the capacitance increase due to the relatively small portion of the etching stop pattern 37a that remains is reduced. --

Please amend the paragraph beginning on page 7, line 21 as follows:

-- The fourth interlayer insulating layer 41 is formed with any one selected from the group consisting of a HDP-USG layer, an undoped silicate layer deposited by the HDP, and an oxide layer deposited by the PECVD method or low pressure chemical vapor deposition method(LPCVD), and the fourth interlayer insulating layer 41 is formed at with a thickness ranging from about 2000 Å to about 30000 Å, in order to form a the void (B) ~~is formed in the via hole 39~~ in the fourth interlayer insulating layer 41 as shown in Fig. 3D. --

Please re-amend the paragraph beginning on page 9, line 5, as follows:

-- Since the remaining portion of the etching stop layer 37a that surrounds the ~~trench~~ via hole 39 (see Figs. 3C-3E) is formed by patterning the etching stop layer 37 (Figs 3B and 3C) so that the layer 37 remains only around the inlet of the via hole 39 (Figs. 3B and 3C), an increase in capacitance due to a larger remaining etching stop layer having high capacitance as shown in Figs. 2A-2B can be prevented. Also, since the interlayer insulating layer 41 having a void is etched to form the trench (Figs. 3D-3E), a margin of a trench etching process may be maximized the etch profile of the resulting structure shown in Fig. 3E is improved over that of the prior art structure shown in Fig. 2B. --